A High-Efficiency Single-Supply RFIC PHS Linear Power Amplifier with Low Adjacent Channel Power Leakage

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ABSTRACT

We present the results and simulation for two 1.9GHz GaAs RFIC power amplifiers. Operated from a single 3.0V supply at a power added efficiency of 40%, these RFIC's produce +25 and +27 dBm output power, respectively, at -57 dBc adjacent channel power from a 384 kbps π/4-DQPSK modulated carrier at 600 kHz offset. When operating in a saturated mode the same RFIC's have an output power greater than 26.5 and 28dBm respectively at over 45% PAE which makes them very attractive for the saturated output applications. We believe this is the best performance reported to date for PHS/PACS mode operation using a single supply RFIC monolithic power amplifier The design technique, including simulation of spectral regrowth based on AM-AM and AM-PM characteristics, are presented for these amplifiers.

INTRODUCTION

Since the introduction of digital modulation schemes in personal communication services there has been a strong need for quasi-linear power amplifiers with good efficiency to insure long talk time between battery charges. The dynamic signal envelope of the π/4-DQPSK modulated carrier at 1.9GHz for the PHS/PACS standard imposes difficult design constraints on traditional high efficiency power amplifier design approaches [1]. In addition, to reduce parts count and handset complexity, the market is also demanding that these power amps operate from a single positive 3V supply with comparable linearity and efficiency to designs that require a negative bias.

This paper discusses the design and performance of a two-stage GaAs radio-frequency integrated circuit (RFIC) power amplifier that requires only a single positive supply The simulation of spectral regrowth based on AM-AM and AM-PM characteristics are presented to demonstrate a very useful design approach for these quasi-linear amplifiers[2] The design utilizes depletion mode GaAs MESFET's operating at 0 V V_{GS} Thus, a single 3 V supply powers the near class A RFIC's. We believe this to be record performance for single supply PHS/PACS standard designs. In addition, the results are very comparable to dual supply designs in performance. Figure 1 compares industry performance to date for this application for both dual and single supply designs operating in the 3V range. As shown in Figure 1 Chip A achieves 25dBm output power (Pout) at 40% power added efficiency (PAE) and Chip B achieves 27dBm Pout at 40% PAE while still meeting -57dBc adjacent channel power (ACP) leakage for the PHS/PACS application. Although the power levels reported are over twice as high as the industry bench marks, the designs reported here can be scaled down in power.

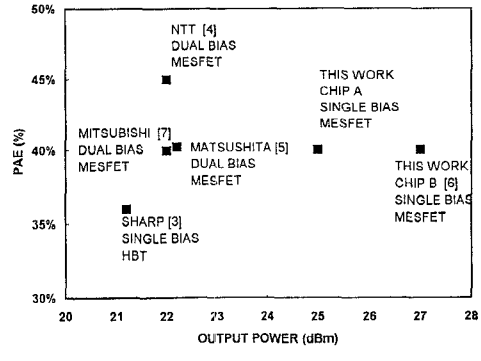

Figure 1: PHS/PACS industry performance for ACP< -55dBc at 600khz offset

TECHNOLOGY

The wafers are manufactured using a standard ion implant recess gate MESFET process with a nominal 0.5um gate length, 20GHz Ft, threshold voltage of -0.6V, and a breakdown of 15V. Passive structures include layers of stackable gold interconnect metal dielectric and a very high density capacitor. These features allow very compact and high density circuitry which help to minimize die cost. The wafer surface is completely encapsulated in dielectric and the wafers are thinned down to 4mils thick and back metalized

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DESIGN

The two RFIC's discussed in this paper are so similar that only the design details for chip B will be discussed. Chip A is a simple scaling of chip B to lower output power that preserves PAE at the same ACP. The design goals for the chip B RFIC were to achieve a saturated output power of 28dBm with a single positive 3V supply from 1880MHz to 1990MHz at > 40% PAE. The MMIC must function in a commercially available 8 pin SOIC plastic package with integral heat sink for both electrical ground and thermal management to maintain a channel temperature less than 150 °C for all operating conditions. Components external to the package are encouraged when they are deemed worthy in a cost/performance trade off or if they allow useful application flexibility. Some examples of useful application flexibility are conditional stability vs. unconditionally stable operation (less gain), filtering trade offs and matching network trade offs.

To simulate the performance FET models were developed and implemented in the LIBRA™ harmonic balance simulator. Initially the Statz [8] model was extracted from a 1200um common source FET for saturated mode simulation where linearity performance is not considered. The standard DC-IV curves and s-parameters over bias were measured and used to get a starting point for the model. To deduce the actual dynamic (>10MHz) current voltage relationship various output loads were hung on the 1200um FET. Output power was tested for these loads and used to refine the dynamic IV curves of the FET model. Although it predicts saturated power well, the Statz model has discontinuities near pinch off in drain current and voltage variable model capacitances. These discontinuities create inaccuracies in simulations of AM-PM phase distortion. To overcome this problem we use a model a which incorporates accurate voltage variable capacitances and drain current near and into threshold to simulate AM-PM and AM-AM performance.

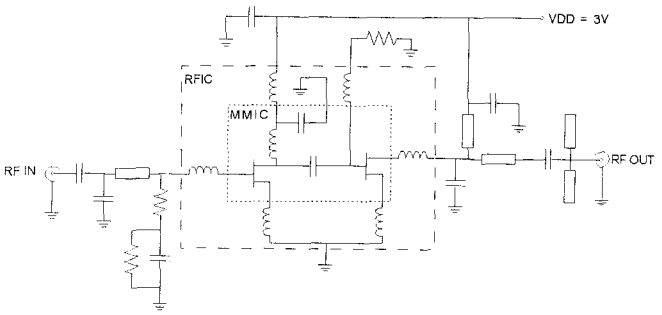

Figure 2: Schematic drawing of the chip B MMIC, RFIC and board design (PM2112).

The power amplifier design is a two-stage common-source power amplifier MMIC with external to the package input and output matching networks (Figure 2). The driver FET gate width is 900 μm, and the output FET is 7.5 mm for the chip B design. The gates are grounded with resistive terminations for stability and bias setting. The input network is chosen to be off chip for application flexibility as discussed above. The output network is off chip because both the cost of these components and electrical losses are high on GaAs. Interstage matching provides for optimum gain at a 1.92 GHz center frequency by providing an impedance transformation from the relatively high output impedance of the first FET to the very low impedance of the 2nd stage FET input. The package (8 pin SOIC with integral heat sink) lead inductances are included in the simulation model and absorbed into matching networks. The chip layout is shown in Figure 3 and the die size is 34 mils by 29 mils.

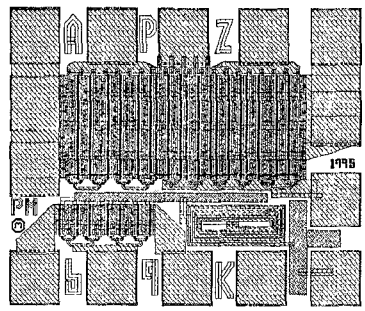

Figure 3: MMIC layout for chip B.

The matched power amplifier circuit was simulated using LIBRA™ to predict the AM-AM and AM-PM performance, shown in Figure 4. Notice that the phase deviation is less than 2° at an output power 1dB compression. The corresponding measured and modeled output power and efficiency is shown in Figure 5. Good agreement is seen between the measured and modeled curves. To predict the ACP for a π/4-DQPSK modulated signal, the AM-AM and AM-PM generated by the LIBRA™ model were fed into an algorithm developed to study intermodulation distortion in power amplifiers [2]. Basically, the procedure consists of calculating the envelope transfer characteristics from the LIBRA™ generated AM-AM and AM-PM characteristics using the Bessel-Fourier transform. A behavioral model is derived from the envelope transfer characteristic, and used to predict the nonlinear distortion on the π/4-DQPSK modulated signal [9]. The ACP is calculated by integrating the simulated output spectrum generated by the algorithm. The algorithm is implemented in MathCAD™, and takes about 2 minutes to compute ACP for a 250 symbol π/4-DQPSK sequence. The resulting ACP shows good agreement compared to the measured ACP for the chip B design (Figure 6).

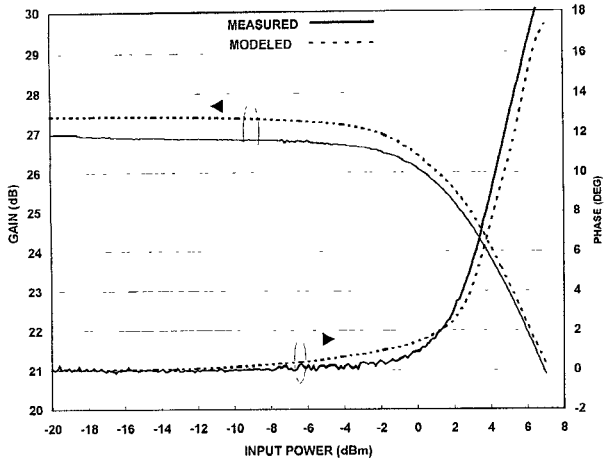

Figure 4. Simulated and measured AM-AM and AM-PM performance.

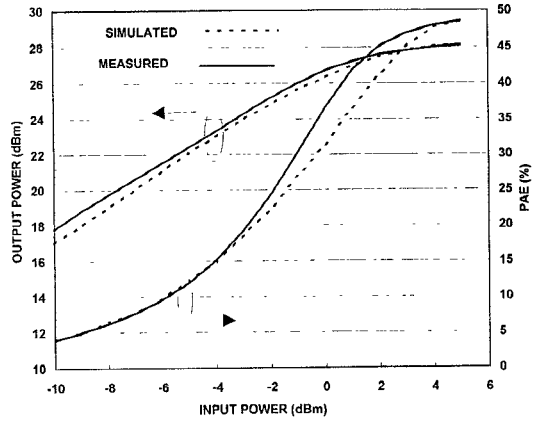

Figure 5. Measured and simulated output power , PAE for chip B.

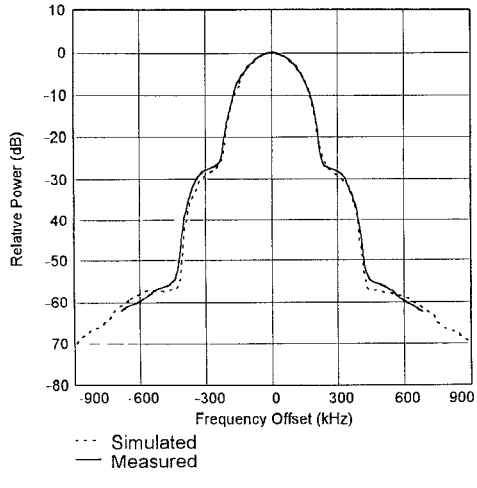

Figure 6: Chip B measured and simulated ACP in the symbol rate bandwidth. Output power = 27dBm at 40% PAE.

RESULTS

The RFIC is soldered to a standard FR4 microstrip board with commercially available chip capacitors and resistors compatible with surface mount techniques. Measurement data includes coax to microstrip connector losses. Figure 7 shows the measured output power, power added efficiency and supply current versus input power for Chip B. When operating in a saturated mode, an output power greater 28dBm at over 45% PAE is achieved. The ACP performance is shown in Figure 6. As is seen, the ACP at 600 kHz offset for a 384 kbps $\pi/4$-DQPSK signal is less than -57 dBc at a channel power of +27 dBm. At this power level, the PAE is 40%, as seen on Figure 6. Figure 8 shows the ACP and PAE over output power for chip B. As shown in Figure 9, Chip A achieves 25dBm output power (Pout) at 40% power added efficiency (PAE) and Chip B achieves 27dBm Pout at 40% PAE while still meeting -57dBc adjacent channel power (ACP) leakage for the PHS/PACS application. The input return loss is better than -10dB over the 1880-1990mhz band. When operated at this gain level and in small signal mode the amplifier is conditionally stable.

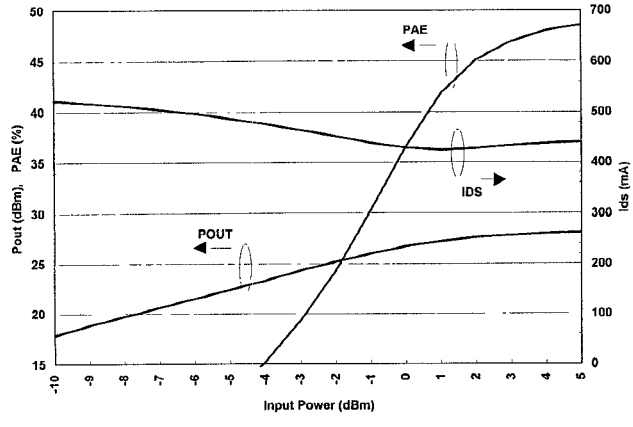

Figure 7 Chip B output power , PAE and drain current.

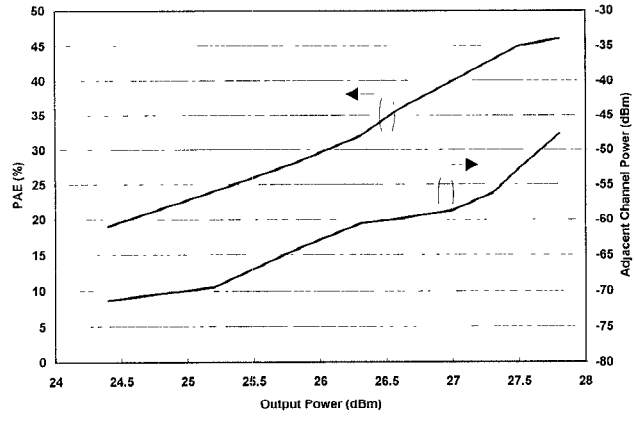

Figure 8: Chip B ACP and PAE vs. output power.

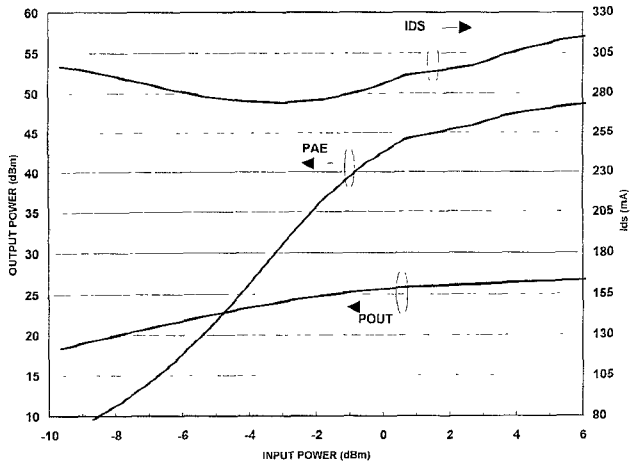

Figure 9. Chip A output power, PAE and Idrain current

CONCLUSIONS

We have presented the results of a two-stage single-supply GaAs RFIC power amplifier for 1 9 GHz operation The design procedure consisted of circuit level simulation using LIBRA™ to predict output power, power-added efficiency, gain compression, and AM-PM distortion. The gain compression and AM-PM simulations are used to generate a behavioral model, which in turn predicts the adjacent channel power (ACP) performance of the power amplifier. The resulting design showed good agreement with the simulated performance The power added efficiency achieved by two different amplifiers is 40%, which is thought to be the best reported to date for a single-supply RFIC power amplifier meeting the PHS/PACS ACP specifications

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